



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,998	05/04/2001	James S. Chapple	42390.P9943	8977

7590 05/16/2003

John P. Ward
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER

PATEL, NIKETA I

ART UNIT PAPER NUMBER

2182

DATE MAILED: 05/16/2003

5

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Office Action Summary

Application No.

09/848,998

Applicant(s)

CHAPPLE ET AL.

Examiner

Niketa I. Patel

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: This application does not contain a brief summary of the disclosure. Appropriate correction is required.

Applicant is reminded of a proper content of a brief summary: Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Art Unit: 2182

3. Claims 1-5 and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirairi U.S. Patent Number: 6,480,942 (hereinafter referred to as "*Hirairi*").

4. Referring to claims 1 and 20, *Hirairi* teaches an apparatus and a method comprising: a queue (see column 5 – lines 34-42); an event selection logic unit (see figure 6 – element 11) to receive a queue enter signal (see figure 6 – element "WRITE ENABLE"), a queue exit signal (see figure 6 – element "READ ENABLE"), and a queue not empty signal from the queue (see figure 6 – elements 11, 16, 15); and a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a decrement event signal delivered by the event selection logic unit (see figure 6 – element 14; column 9 – lines 63-67; column 10 – 1-28).

5. Referring to claim 2, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal (see figure 6 – elements 11, 16, 15).

6. Referring to claim 3, *Hirairi* teaches further comprising a data register coupled to the counter (see figure 6 – elements "CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES", "CONSTANT: 0"; column 10 – lines 55-67; column 11 – lines 1-8).

7. Referring to claims 4 and 22, *Hirairi* teaches an apparatus and a method further comprising a comparator (see figure 7A – element 14; figure 7B – elements 1B, 1A) including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event selection logic unit (see figure 7A – element 14; figure 7B – elements 1B, 1A; column 11 – lines 12-38).

8. Referring to claim 5, *Hirairi* teaches that the event selection logic including programmable function to allow a variety of combinations of the queue enter, queue exit, queue

Art Unit: 2182

not empty, and comparator output signals to serve as increment or decrement events (see figure 6 – elements 1, 11, 16, 15; column 9 – lines 63-67; column 10 – lines 1-28).

9. Referring to claim 6, *Hirairi* teaches further comprising a block of registers including a command register and a status register (see figure 6 – elements 12, 13, 14, 16, 15, 18, 17).

10. Referring to claim 21, *Hirairi* teaches further comprising storing the counter value in a data register (see figure 6 – elements 14, 16, 15; column 9 – lines 63-67; column 10 – lines 1-67; column 11 – lines 1-55).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 7-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Hirairi* U.S. Patent Number: 6,480,942 (hereinafter referred to as “*Hirairi*”).

Art Unit: 2182

14. Referring to claims 7 and 12, *Hirairi* teaches a queue (see column 5 – lines 34-42), an event selection logic unit (see figure 6 – element 11) to receive a queue enter signal (see figure 6 – element “WRITE ENABLE”), a queue exit signal (see figure 6 – element “READ ENABLE”), and a queue not empty signal from the queue (see figure 6 – elements 11, 16, 15); and a first counter to increment in response to a first increment event signal delivered by the event selection logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event selection logic unit (see figure 6 – element 14; column 9 – lines 63-67; column 10 – 1-28). *Hirairi* fails to explicitly set forth the limitation of a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit and the second counter to increment in response to the comparator output indication that the first counter value matches the data register value.

One of ordinary skill in the art at the time of applicant’s invention would have clearly recognized that it is quite advantageous for the FIFO control system of *Hirairi* to have a second counter to increment in response to a increment signal and decrement in response to decrement signal to allow for a second FIFO read and write functions to be recorded. It is for this reason that one of ordinary skill in the art would have been motivated to implement a second counter to a increment signal and decrement in response to decrement signal to allow a FIFO entry and exit functions to be recorded.

15. Referring to claim 8, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal (see figure 6 – elements 11, 16, 15).

Art Unit: 2182

16. Referring to claim 9, *Hirairi* teaches further comprising a data register coupled to the first counter (see figure 6 – elements “CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES”, “CONSTANT: 0”; column 10 – lines 55-67; column 11 – lines 1-8).

17. Referring to claim 10, *Hirairi* teaches further comprising a comparator (see figure 7A – element 14; figure 7B – elements 1B, 1A) including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event selection logic unit (see figure 7A – element 14; figure 7B – elements 1B, 1A; column 11 – lines 12-38).

18. Referring to claim 11, *Hirairi* teaches the event selection logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events (see figure 6 – elements 1, 11, 16, 15; column 9 – lines 63-67; column 10 – lines 1-28).

19. Referring to claim 13, *Hirairi* teaches further comprising a block of registers including a command register and a status register (see figure 6 – elements 12, 13, 14, 16, 15, 18, 17).

20. Referring to claim 14, *Hirairi* teaches a queue (see column 5 – lines 34-42); an event selection logic unit (see figure 6 – element 11) to receive a queue enter signal (see figure 6 – element “WRITE ENABLE”), a queue exit signal (see figure 6 – element “READ ENABLE”), and a queue not empty signal from the queue (see figure 6 – elements 11, 16, 15); and a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a decrement event signal delivered by the event selection logic unit (see figure 6 – element 14; column 9 – lines 63-67; column 10 – 1-28). *Hirairi* fails to explicitly set forth the limitation of system with a processor. It would have been obvious to one

Art Unit: 2182

of ordinary skill in the art at the time of applicant's invention that a processor was old and well known in the computer art to be used with FIFO system to allow the data in the FIFO system to be processed. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to implement *Hirairi's* invention to include a processor to process data within the FIFO system.

21. Referring to claim 15, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal (see figure 6 – elements 11, 16, 15).

22. Referring to claim 16, *Hirairi* teaches further comprising a data register coupled to the counter (see figure 6 – elements “CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES”, “CONSTANT: 0”; column 10 – lines 55-67; column 11 – lines 1-8).

23. Referring to claim 17, *Hirairi* teaches further comprising a comparator (see figure 7A – element 14; figure 7B – elements 1B, 1A) including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event selection logic unit (see figure 7A – element 14; figure 7B – elements 1B, 1A; column 11 – lines 12-38).

24. Referring to claim 18, *Hirairi* teaches that the event selection logic including programmable function to allow a variety of combinations of the queue enter, queue exit, queue not empty, and comparator output signals to serve as increment or decrement events (see figure 6 – elements 1, 11, 16, 15; column 9 – lines 63-67; column 10 – lines 1-28).

25. Referring to claim 19, *Hirairi* teaches further comprising a block of registers including a command register and a status register (see figure 6 – elements 12, 13, 14, 16, 15, 18, 17).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to gathering queue performance.

Holden U.S. Patent Number: 6,134,218

Kamaraj et al. U.S. Patent Number: 6,501,757

Rossum U.S. Patent Number: 6,092,126

Noeldner et al. U.S. Patent Number: 6,449,666


Erimli et al. U.S. Patent Number: 6,487,212

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 9:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746 7239 for regular communications and (703) 746 7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

NP
May 2, 2003


JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Application/Control Number: 09/848,998

Page 9

Art Unit: 2182